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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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PERKINS COIE LLP			TRAN, LONG K	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/756,051	Applicant(s) JENG, ERIK S.	
	Examiner Long K. Tran	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 19 - 30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 19 - 30 is/are rejected.
- 7) ☒ Claim(s) 19, 24 and 26 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 January 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date. _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of **Group II, claims 19 – 30** and applicant's cancellation of Group I, claims 1 – 18 and Group III, claims 31 – 34 in the reply filed on May 12, 2003 is acknowledged.
2. Claims **19 – 30** are presented for examination.

Drawings

3. The drawings, figures 1A, 2A, 2D, 2E and 2G, are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters are pointed to wrong elements. For example, in figure 1A, character 104 not pointed to source/drain, in figure 2A, character 202 pointed to conductor layer... . Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.
4. Figure 1A – 1C should be designated by a legend such as --Prior Art-- (see application specification paragraph [0008]) because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are

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required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

6. The disclosure is objected to because of the following informalities: Paragraph [0018] line 2: change "the present invention" to --prior art--.

7. Abstract: line 1, suggest changing "comprises" to --includes--.

Appropriate correction is required.

Claim Objections

8. Claim **24** is objected to because of the following informalities: the limitation "first" is a typo mistake. The applicant should remove this limitation or amend the claim. For examination purpose: in line 2: delete ", first".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims **19 – 25** and **28 – 30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US Patent No. 5486,480) in view of Liu (US Patent No. 6,468,915).

Regarding claim **19**, Chen discloses a nonvolatile memory, comprising:

a substrate 40 (fig. 5) having source/drain 90 (figs. 9 & 10) at unselected side (Note: this side is covered by a photoresist mask 82 (fig. 8; column 5, lines 65 and 66)) and source/drain 92 (figs. 9 & 10) with source/drain extension 80 (figs. 9 & 10; column 6, lines 5 – 17) formed at other selected side.

gate dielectric layer 52 (figs. 7 – 10; column 5, lines 18 – 20) formed on the substrate 40;

gate structure 54 and 74 – 76 (figs. 7 – 10; column 5, lines 61 and 62);

isolation layers 86 and 88 (figs. 9 & 10; column 6, lines 5 – 7) formed along the side surface of the gate structure 54 and 74 – 76;

spacers 94 and 96 (fig. 10; column 6, line 18). Formed attached on the sidewalls of the isolation layers 86 and 88.

Chen fails to show the isolation layer formed along the surface of the gate.

However, Liu shows oxide layers 52A, 52B (fig. 4C; column 4, lines 58 – 61) formed along the surface of the gate 46 (fig. 4C).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the nonvolatile memory of Chen with the isolation layer

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formed along the surface of the gate as shown by Liu in order to protect the gate and to form a stress buffer under the next deposited silicon nitride layer (column 4, lines 62 – 66).

Regarding claim **20**, Chen in view of Liu discloses the thickness of the gate structure is about 1200Å – 3000Å (Liu: column 4, line 31) but fails to show the thickness of the gate is approximately 800 – 2500Å.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the device of Chen in view of Liu with a gate having thickness of approximately 800 – 2500Å as the instant claim, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art.

Moreover, applicant to be of significant importance for patentability has not alleged the thickness of the gate.

Regarding claim **21**, Chen in view of Liu discloses the thickness of the gate dielectric layer 52 (Chen: fig. 7 – 10; column 5, lines 18 – 20) is about 150Å – 250Å but fails to show the thickness of the isolation layer is approximately 10 – 250Å.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the device of Chen in view of Liu with a gate dielectric layer having thickness of approximately 10 – 250Å as the instant claim, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art.

Moreover, applicant to be of significant importance for patentability has not alleged the thickness of the gate dielectric layer.

Regarding claim **22**, Chen in view of Liu discloses the claimed invention of claim 19 and shows the isolation layer is about 1000 – 1500Å (Liu: column 5, lines 19 – 21) but fails to show the thickness of the isolation layer is approximately 20 – 200Å.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the device of Chen in view of Liu with an isolation having thickness of approximately 20 – 200Å as the instant claim, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art.

Moreover, applicant to be of significant importance for patentability has not alleged the thickness of the isolation layer.

Regarding claim **23**, Chen in view of Liu discloses the spacers 56 (Liu: fig. 4F; column 5, lines 30 – 32) with the width of 200 – 300Å) but fails to show the thickness of the isolation layer is approximately 200 – 2000Å.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the device of Chen in view of Liu with spacers having thickness of approximately 200 – 2000Å as the instant claim, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art.

Moreover, applicant to be of significant importance for patentability has not alleged the thickness of the spacers.

Regarding claim **24**, Chen in view of Liu discloses silicide layer 62A and 62B (Liu: fig. 4H; column 6, lines 7 – 21) on gate 46/47 (note: reference specification shows polysilicon gate 47. However, in figures 4A – 4H, character 46 points direct to polysilicon gate) and on source/drain regions 60 (note: reference specification shows source/drain regions 560. However, in figure 4H, character 60 used to designate source/drain regions)

Regarding claim **25**, Chen in view of Liu discloses the gate dielectric layer includes silicon dioxide (Chen: column 5, lines 18 – 20).

Regarding claim **28**, Chen in view of Liu discloses the spacers 56 (Liu: fig. 4H; column 5, line 27) are formed of silicon nitride.

Regarding claim **29**, Chen in view of Liu discloses the ion source for the sour/drain 90 and 92 (Chen: figs. 9 and 10; column 6, lines 7 – 17) is phosphorus.

Regarding claim **30**, Chen in view of Liu discloses the pocket ion implantation region 80 (Chen: figs 9 and 10) formed adjacent to the source/drain 92 and gate structure 54 and 74 – 76, wherein the conductive type (Chen: p-type; column 5, lines 63 – 65) of the pocket ion implantation region is opposite to the one of the source/drain (Chen: n-type; column 6, lines 7 and 8).

11. Claims **26** and **27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US Patent No. 5486,480) in view of Liu (US Patent No. 6,468,915) and further in view of Clevenger et al. (US Patent Application Publication No. 2002/0163039).

Regarding claims **26** and **27**, Chen in view of Liu discloses the claimed invention of claims 19 and 25 except for the gate dielectric layer includes the material with high dielectric constant around 3 – 100; and is selected from Ta₂O₅, Al₂O₃, ZrO₂, Gd₂O₃ or Y₂O₃.

However, Clevenger shows the gate dielectric layer 20 (fig.1; [0006] and [0023]) comprising high-k dielectric such as Al₂O₃ or Ta₂O₅ (tantalum oxide having a dielectric constant of 11.6; See attached pages from:
http://www.clippercontrols.com/info/dielectric_constant.html.)

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the gate dielectric of Chen with the high k material gate dielectric layer such as Al₂O₃ or Ta₂O₅ shown by Clevenger in order to lower the gate conductor leakage ([0006]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LKT

July 22, 2005

LKTRM